19-3690; Rev 0; 6/05

EVALUATION KIT AVAILABLE

High-Efficiency, 10A, PWM Internal-Switch Step-Down Regulator

MAX8566

General Description

The MAX8566 high-efficiency switching regulator delivers up to 10A load current at output voltages from 0.6V to (0.87 x V_{IN}). The IC operates from 2.3V to 3.6V input supplies, making it ideal for point-of-load applications. The total output-voltage set error is less than ±1% over load, line, and temperature.

The MAX8566 operates in pulse-width-modulation (PWM) mode with a 250kHz to 2.4MHz switching frequency range that is programmable by an external resistor. The IC can be synchronized to an external clock in the same frequency range using the SYNC input. The high operating frequency minimizes the size of external components. Using low-$R_{DS(ON)}$ n-channel MOSFETs for both high- and low-side switches maintains high efficiency at both heavy-load and high-switching frequencies.

The MAX8566 employs a voltage-mode control architecture with a high-bandwidth (> 10MHz) error amplifier. The voltage-mode control architecture makes switching frequencies greater than 1MHz possible, achieving all-ceramic-capacitor designs to minimize PC board space. The error amplifier works with Type 3 compensation to fully utilize the bandwidth of the high-frequency switching to obtain fast transient response. Adjustable soft-start time provides flexibility to minimize input startup inrush current. An open-drain, power-good (PWRGD) signal goes high when the output reaches 90% of its regulation point.

The MAX8566 provides a SYNCOUT output to synchronize a second MAX8566 or a second regulator switching 180° out-of-phase with the first to reduce the input ripple current, which consequently reduces the input-capacitance requirements. The MAX8566 also provides an external reference input (REFIN) for output-tracking applications.

The MAX8566 is available in a 32-pin, 5mm x 5mm thin QFN package. The MAX8566 and all the required external components fit into a footprint of less than 0.80in^2.

Applications

ASIC/CPU/DSP Core Voltages

POL Power Supplies

DDR Power Supplies

Base-Station Power Supplies

Fiber Power Supplies

Telecom Power Supplies

Network Power Supplies

Features

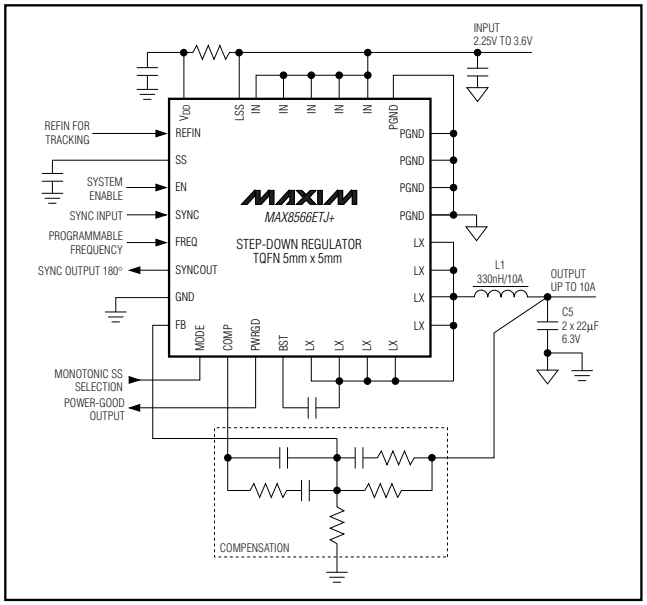
- ♦ **Internal 8mΩ On-Resistance MOSFETs**
- ♦ **10A Output PWM Step-Down Regulator**
- ♦ **±1% Output Accuracy over Load, Line, and Temperature**
- ♦ **Operates from 2.3V to 3.6V Input Supply**
- ♦ **Adjustable Output from 0.6V to (0.87 x V_{IN})**
- ♦ **250kHz to 2.4MHz Adjustable Frequency or SYNC Input**
- ♦ **Allows All-Ceramic-Capacitor Design**
- ♦ **SYNCOUT Drives 2nd Regulator 180° Out-of-Phase**
- ♦ **Prebiased or Monotonic Soft-Start**
- ♦ **Programmable Soft-Start Time**
- ♦ **Output Tracking or Sequencing**
- ♦ **Sourcing and Sinking Output Current**
- ♦ **Power-Good Output**
- ♦ **32-Lead Thin QFN Package**
- ♦ **REFIN for DDR-Termination Application**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8566ETJ+	-40°C to +85°C	32 Thin QFN 5mm x 5mm (T3255-4)

+Denotes lead-free package.

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

EN/SS, EN, IN, SYNC, SKIP, V_{DD}, LSS, PWRGD to GND .....-0.3V to +4V (4.5V nonswitching)
SYNCOUT, SS, COMP, FB, REFIN, FREQ to GND .....-0.3V to (V_{DD} + 0.3V)
LX Current (Note 1).....-12A to +12A
BST to LX.....-0.3V to +4V (4.5V nonswitching)
PGND to GND .....-0.3V to +0.3V

Continuous Power Dissipation (T_A = +85°C)
32-Pin Thin QFN (derate 33.3mW/°C above +70°C).....2666.7W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX has internal clamp diodes to PGND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power-dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{DD} = V_{EN} = 3.3V, V_{FB} = 0.5V, V_{SYNC} = 0V, **T_A = 0°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN/V_{DD}						
IN and V_{DD} Voltage Range			2.3		3.6	V
LSS Voltage Range			2.3		3.6	V
IN Supply Current	Quiescent current, V_{FB} = 0.7V			0.7	2.2	mA
	f_S = 1MHz, no load			14		
V_{DD} Supply Current	Quiescent current, V_{FB} = 0.7V			1.8	4	mA
	f_S = 1MHz, V_{LSS} = V_{DD}			16		
Total Shutdown Current into IN and V_{DD}	V_{IN} = V_{DD} = V_{LSS} = (V_{BST} - V_{LX}) = 3.6V, V_{EN} = 0V	T_A = +25°C			50	µA
		T_A = 0°C to +85°C		3		
V_{DD} Undervoltage-Lockout Threshold	LX starts/stops switching, 2µs deglitch	V_{DD} rising		2.0	2.2	V
		V_{DD} falling	1.72	1.90		
BST						
Shutdown Supply Current	V_{IN} = V_{DD} = V_{BST} = 3.6V, V_{LX} = 3.6V or 0V, V_{EN} = 0V	T_A = +25°C			10	µA
		T_A = 0°C to +85°C		0.05		
PWM COMPARATOR						
Comparator Propagation Delay	10mV overdrive			20		ns
COMP						
Clamp Voltage, High	V_{IN} = 2.3V to 3.6V, V_{FB} = 0.7V		1.80	2.0	2.15	V
Slew Rate			0.75	1.4		V/µs
Shutdown Resistance	From COMP to GND, V_{EN} = 0V			30	100	Ω
ERROR AMPLIFIER						
FB Regulation Voltage	V_{COMP} = 1V to 2V, V_{DD} = 2.5V and 3.3V		0.594	0.6	0.606	V
Error-Amplifier Common-Mode Input Range	V_{DD} = 2.3V to 2.6V		0		V_{DD} - 1.65	V
	V_{DD} = 2.6V to 3.6V		0		V_{DD} - 1.7	
Error-Amplifier Maximum Output Current			0.8			mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = V_{EN} = 3.3V, V_{FB} = 0.5V, V_{SYNC} = 0V, **T_A = 0°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FB Input Bias Current	V_{FB} = 0.7V, T_A = +25°C			40	200	nA
REFIN Input Bias Current	V_{REFIN} = 0.6V, T_A = +25°C			70	250	nA
REFIN Common-Mode Range	V_{DD} = 2.3V to 2.6V		0		V_{DD} - 1.65	V
	V_{DD} = 2.6V to 3.6V		0		V_{DD} - 1.7	
LX (ALL PINS COMBINED)						
On-Resistance, High Side	I_{LX} = -2A	V_{IN} = V_{BST} - V_{LX} = 3.3V		8	16	mΩ
		V_{IN} = V_{BST} - V_{LX} = 2.5V		12	20	
On-Resistance, Low Side	I_{LX} = 2A	V_{IN} = V_{LSS} = 3.3V		8	16	mΩ
		V_{IN} = V_{LSS} = 2.5V		12	20	
Current-Limit Threshold	V_{IN} = 2.5V or 3.3V, high side		12	15	20	A
Leakage Current	V_{IN} = 3.6V, V_{EN} = 0V, T_A = +25°C	V_{LX} = 3.6V		5	200	µA
		V_{LX} = 0V	-200	+5		
Switching Frequency	V_{IN} = 2.5V or 3.3V	R_{FREQ} = 50kΩ	0.8	1	1.2	MHz
		R_{FREQ} = 23.3kΩ	1.7	2	2.3	
Minimum Off-Time	V_{IN} = 2.5V or 3.3V			50	75	ns
Maximum Duty Cycle	R_{FREQ} = 50kΩ, V_{IN} = 2.5V or 3.3V		87	95		%
Minimum Duty Cycle	R_{FREQ} = 50kΩ, V_{IN} = 2.5V or 3.3V			10		%
RMS LX Output Current					10	A
ENABLE/SOFT-START						
EN Input Logic-Low Threshold				0.4	0.7	V
EN Input Logic-High Threshold			1.65	1.90		V
MODE Input Threshold	V_{DD} = 2.3V to 3.6V	Monotonic start	30		45	% of V_{DD}
		No monotonic start			20	
EN, MODE Input Current	V_{EN} = V_{MODE} = 0V or 3.6V, V_{DD} = 3.6V, T_A = +25°C			0.01	1	µA
Soft-Start Charging Current	V_{SS} = 0.3V		5	8	11	µA
SS Discharge Resistance				8		kΩ

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = V_{EN} = 3.3V, V_{FB} = 0.5V, V_{SYNC} = 0V, **T_A = 0°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC						
Capture Range	V_{DD} = 2.3V to 3.6V		0.25		2.40	MHz
Pulse Width	V_{DD} = 2.3V to 3.6V	t_{LO}	100			ns
		t_{HI}	100			
Input Threshold	V_{DD} = 2.3V to 3.6V	V_{IH}	0.4	0.95		V
		V_{IL}		1	1.6	
Input Current	V_{SYNC} = 0V or 3.6V, V_{DD} = 3.6V	I_{IH}	-1		+10	µA
		I_{IL}, T_A = +25°C	-1	+0.01	+1	
SYNCOUT						
Frequency Range	V_{DD} = 2.3V to 3.6V		0.25		2.40	MHz
Phase Shift from SYNC or Internal Oscillator	Frequency = 1MHz		160	180	230	Degrees
Output Voltage	$I_{SYNCOUT}$ = ±1mA, V_{DD} = 2.3V to 3.6V	V_{OH}	V_{DD} - 0.4	V_{DD} - 0.05		V
		V_{OL}		0.05	0.4	
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	When LX stops switching			+165		°C
Thermal-Shutdown Hysteresis				20		°C
POWER GOOD						
Threshold Voltage	V_{FB} falling, 3mV hysteresis		86	90	93	% of V_{REFIN} or 0.6V
Falling-Edge Deglitch			30	50	80	µs
Output Low Voltage	I_{PWRGD} = 4mA			0.15	0.3	V
Leakage Current	V_{PWRGD} = 3.6V, V_{FB} = 0.9V, T_A = +25°C			0.01	1	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{DD} = V_{EN} = 3.3V, V_{FB} = 0.5V, V_{SYNC} = 0V, **T_A = -40°C to +85°C**, unless otherwise noted. Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN/V_{DD}						
IN and V_{DD} Voltage Range			2.325		3.600	V
LSS Voltage Range			2.325		3.600	V
IN Supply Current	Quiescent current, V_{FB} = 0.7V				2.2	mA
V_{DD} Supply Current	Quiescent current, V_{FB} = 0.7V				4	mA
V_{DD} Undervoltage-Lockout Threshold	LX starts/stops switching, 2µs rising/falling-edge delay	V_{DD} rising			2.2	V
		V_{DD} falling	1.72			
COMP						
Clamp Voltage, High	V_{IN} = 2.3V to 3.6V, V_{FB} = 0.7V		1.80		2.18	V
Slew Rate			0.75			V/µs
Shutdown Resistance	From COMP to GND, V_{EN} = 0V				100	Ω
ERROR AMPLIFIER						
FB Regulation Voltage	V_{COMP} = 1V to 2V, V_{IN} = 2.3V or 3.6V		0.591		0.609	V
Error-Amplifier Common-Mode Input Range	V_{DD} = 2.325V to 2.6V		0		V_{DD} - 1.65	V
	V_{DD} = 2.6V to 3.6V		0		V_{DD} - 1.7	
Error-Amplifier Maximum Output Current			0.8			mA
REFIN Common-Mode Range	V_{DD} = 2.325V to 2.5V		0		V_{DD} - 1.65	V
	V_{DD} = 2.6V to 3.6V		0		V_{DD} - 1.7	
LX (ALL PINS COMBINED)						
On-Resistance, High Side	I_{LX} = -2A	V_{IN} = V_{BST} - V_{LX} = 3.3V			16	mΩ
		V_{IN} = V_{BST} - V_{LX} = 2.5V			20	
On-Resistance, Low Side	I_{LX} = 2A	V_{IN} = V_{LSS} = 3.3V			15	mΩ
		V_{IN} = V_{LSS} = 2.5V			20	
Current-Limit Threshold	V_{IN} = 2.5V or 3.3V		12		20	A

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = V_{EN} = 3.3V, V_{FB} = 0.5V, V_{SYNC} = 0V, **T_A = -40°C to +85°C**, unless otherwise noted. Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Frequency	V_{IN} = 2.5V or 3.3V	R_{FREQ} = 50kΩ	0.8		1.2	MHz
		R_{FREQ} = 23.3kΩ	1.7		2.3	
Minimum Off-Time	V_{IN} = 2.5V or 3.3V				90	ns
Maximum Duty Cycle	R_{FREQ} = 50kΩ, V_{IN} = 2.5V or 3.3V		87			%
RMS Output Current					10	A
ENABLE/SOFT-START						
EN Input Logic-Low Threshold					0.7	V
EN Input Logic-High Threshold			1.65			V
MODE Input Threshold	V_{IN} = 2.3V to 3.6V	Monotonic start	30		45	% of V_{DD}
		No monotonic start			20	
EN, MODE Input Current	V_{EN} or V_{MODE} = 0V or 3.6V, V_{DD} = 3.6V				1	µA
Soft-Start Charging Current	V_{SS} = 0.3V		5		12	µA
SYNC						
Capture Range	V_{IN} = 2.3V to 3.6V		0.25		2.40	MHz
Pulse Width	V_{IN} = 2.3V to 3.6V	t_{LO}	100			ns
		t_{HI}	100			
Input Threshold	V_{IN} = 2.3V to 3.6V	V_{IH}	0.4			V
		V_{IL}			1.6	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = V_{EN} = 3.3V, V_{FB} = 0.5V, V_{SYNC} = 0V, **T_A = -40°C to +85°C**, unless otherwise noted. Note 2)

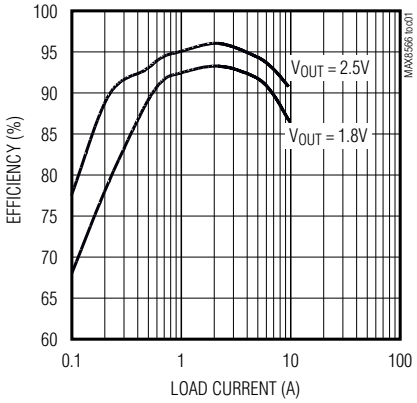
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNCOUT						
Frequency Range	V_{DD} = 2.3V to 3.6V		0.25		2.40	MHz
Phase Shift from SYNC or Internal Oscillator	Frequency = 1MHz		160		230	Degrees
Output Voltage	$I_{SYNCOUT}$ = ±1mA, V_{DD} = 2.3V to 3.6V	V_{OH}	V_{DD} - 0.4			V
		V_{OL}			0.4	
POWER-GOOD						
Threshold Voltage	V_{FB} falling, 3mV hysteresis		85		93	% of V_{REF}
Falling-Edge Deglitch			30		80	µs
PWRGD Output Voltage	I_{PWRGD} = 4mA				0.3	V

Note 2: Specifications to -40°C are guaranteed by design and not production tested.

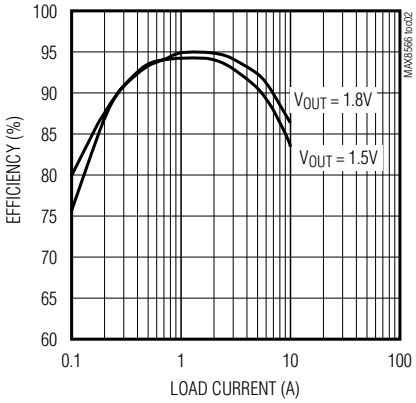
Typical Operating Characteristics

(Typical values are at V_{IN} = V_{DD} = 3.3V, V_{OUT} = 1.8V, R_{FREQ} = 50kΩ, I_{OUT} = 10A, and T_A = +25°C.)

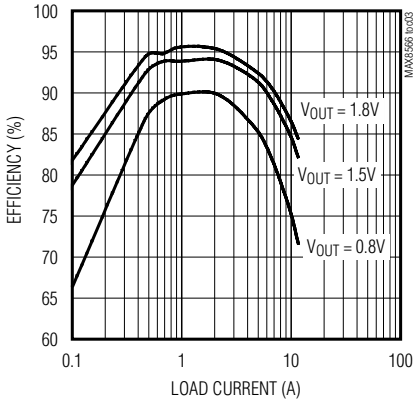
EFFICIENCY vs. LOAD CURRENT
V_{IN} = V_{LSS} = 3.3V



EFFICIENCY vs. LOAD CURRENT
V_{IN} = V_{LSS} = 2.5V



EFFICIENCY vs. LOAD CURRENT
V_{IN} = 2.5V, V_{LSS} = 3.3V

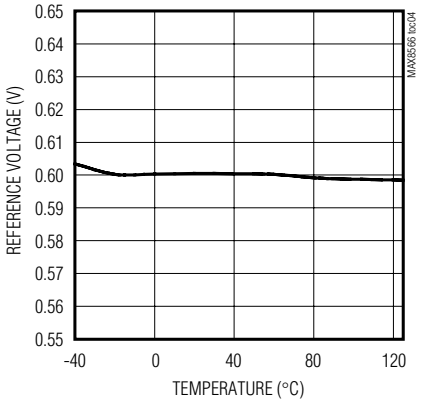


High-Efficiency, 10A, PWM Internal-Switch Step-Down Regulator

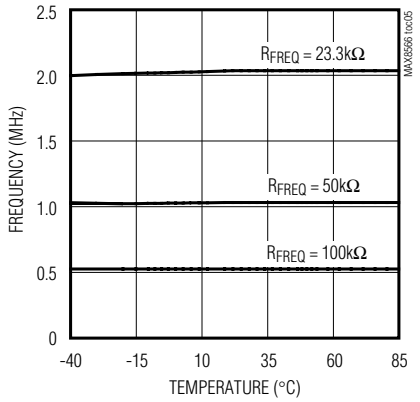
Typical Operating Characteristics (continued)

(Typical values are at V_{IN} = V_{DD} = 3.3V, V_{OUT} = 1.8V, R_{FREQ} = 50kΩ, I_{OUT} = 10A, and T_A = +25°C.)

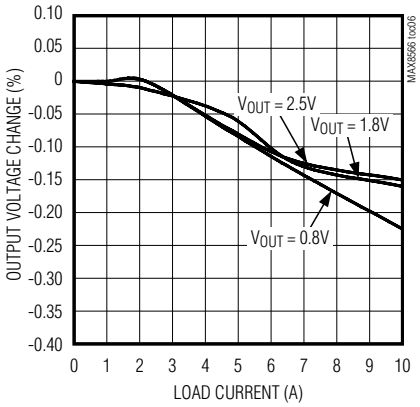
REFERENCE VOLTAGE vs. TEMPERATURE



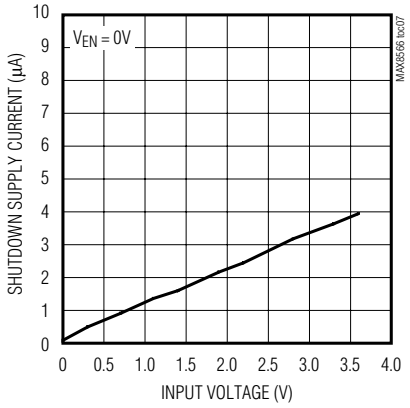
FREQUENCY vs. TEMPERATURE



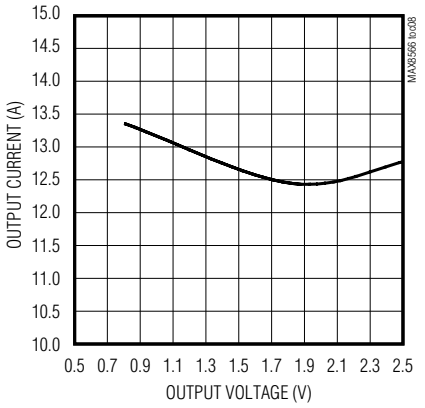
LOAD REGULATION



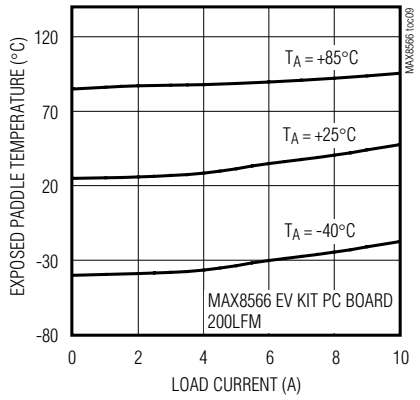
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



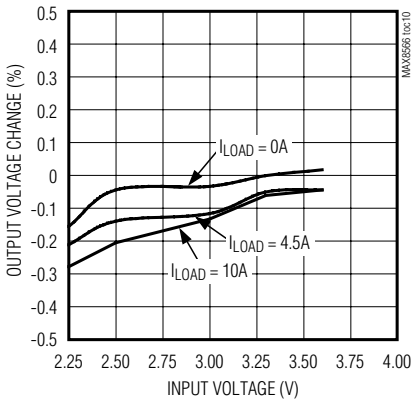
MAXIMUM OUTPUT CURRENT vs. OUTPUT VOLTAGE



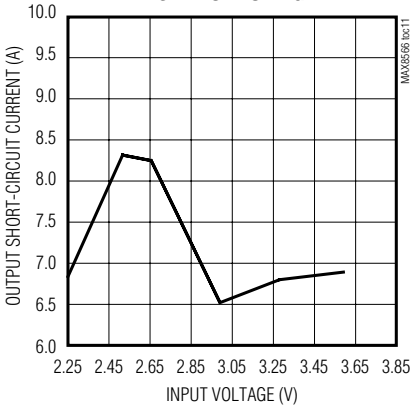
EXPOSED PADDLE TEMPERATURE vs. LOAD CURRENT



LINE REGULATION



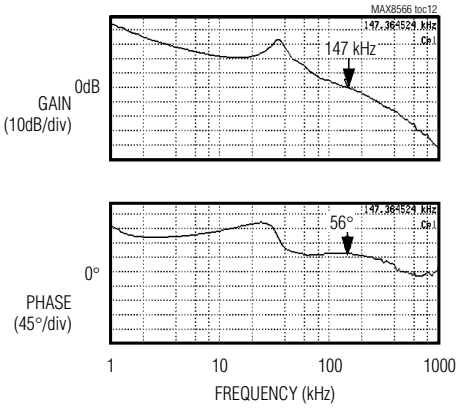
OUTPUT SHORT-CIRCUIT CURRENT vs. INPUT VOLTAGE



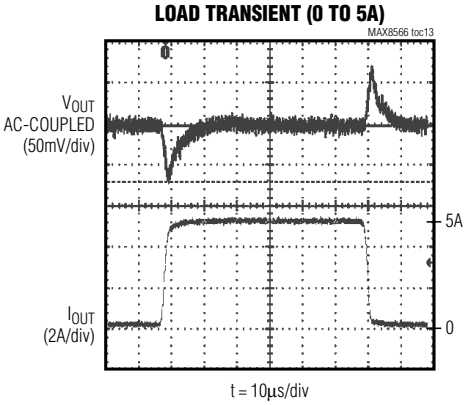
Typical Operating Characteristics (continued)

(Typical values are at V_{IN} = V_{DD} = 3.3V, V_{OUT} = 1.8V, R_{FREQ} = 50kΩ, I_{OUT} = 10A, and T_A = +25°C.)

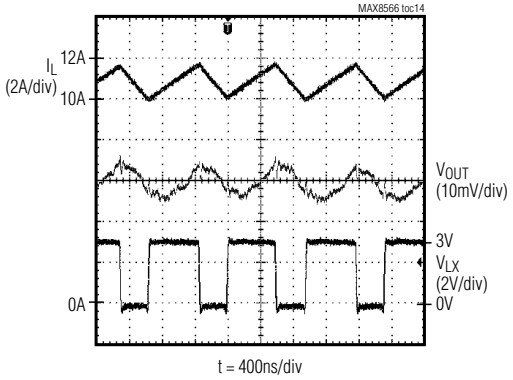
GAIN/PHASE OF THE VOLTAGE LOOP



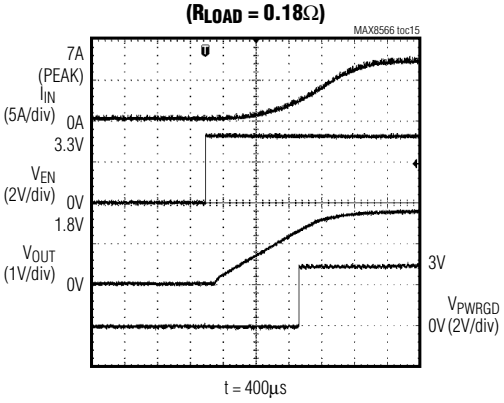
LOAD TRANSIENT (0 TO 5A)



FULL-LOAD SWITCHING WAVEFORMS



STARTUP INTO 0.18Ω LOAD (R_{LOAD} = 0.18Ω)

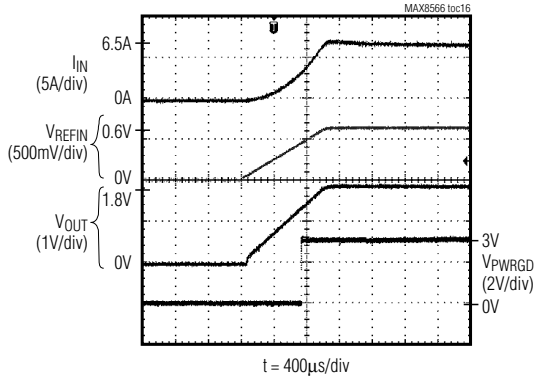


High-Efficiency, 10A, PWM Internal-Switch Step-Down Regulator

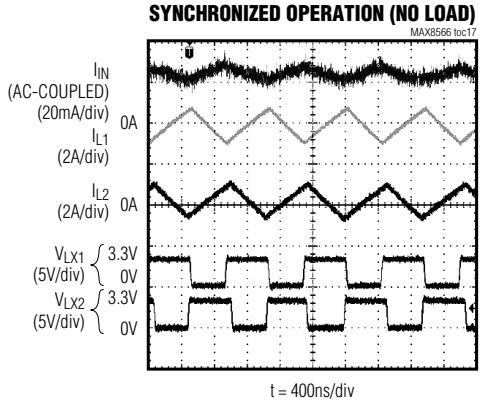
Typical Operating Characteristics (continued)

(Typical values are at V_{IN} = V_{DD} = 3.3V, V_{OUT} = 1.8V, R_{FREQ} = 50kΩ, I_{OUT} = 10A, and T_A = +25°C.)

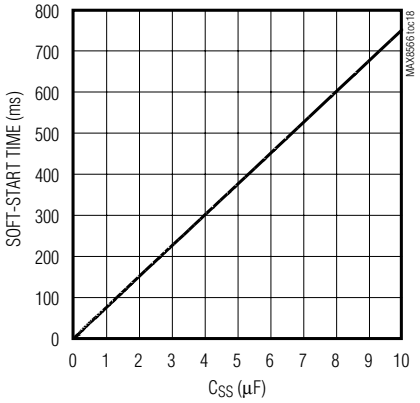
SOFT-START WITH REFIN



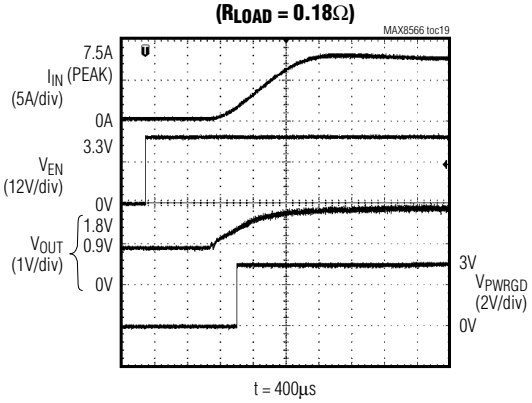
SYNCHRONIZED OPERATION (NO LOAD)



SOFT-START TIME vs. SOFT-START CAPACITANCE



STARTUP INTO PREBIASED OUTPUT (R_{LOAD} = 0.18Ω)



Pin Description

PIN	NAME	FUNCTION
1	MODE	Monotonic Startup Enable/Disable. Connect MODE to GND or to the center tap of an external resistor-divider to enable/disable monotonic startup mode.
2	COMP	Error-Amplifier Output. Connect the necessary compensation network from COMP to FB. COMP is internally pulled to GND when the IC is in shutdown mode.
3	PWRGD	Power-Good Output. Open-drain output that is high impedance when $V_{FB} \geq 90\%$ of 0.6V. Otherwise, PWRGD is internally pulled low. PWRGD is internally pulled low when the IC is in shutdown mode, V_{DD} is below the UVLO threshold, or the IC is in thermal shutdown.
4	BST	High-Side MOSFET Driver Supply. Bypass BST to LX with a 0.1µF capacitor. BST is connected to LSS through an internal pMOS switch.
5–12	LX	Inductor Connection. All LX pins are internally connected together. Connect all LX pins to the switched side of the inductor. LX is high impedance when the IC is in shutdown mode.
13–17	PGND	Power Ground. All PGND pins are internally connected. Connect all PGND pins externally to the power ground plane.
18–22	IN	Input Power Supply. All IN pins are internally connected. Connect all IN pins externally to an input supply from 2.3V to 3.6V. Bypass IN to PGND with 20µF of ceramic capacitance.
23	LSS	Low-Side MOSFET-Driver Supply Voltage. Connect to a 2.3V to 3.6V supply voltage.
24	V_{DD}	IC Supply Voltage Input. Connect V_{DD} to IN through an external 2Ω resistor. Bypass V_{DD} to GND with a 4.7µF capacitor.
25	REFIN	External Reference Input. Connect to an external reference. FB regulates to the voltage at REFIN. Connect REFIN to SS to use the internal reference.
26	SS	Soft-Start Input. Connect a capacitor from SS to GND to set the soft-start time. See the *Soft-Start* section.
27	EN	Enable Input. Active-high logic input to enable/disable the MAX8566. Connect to IN to enable the IC; connect to GND to disable the IC.
28	SYNC	Synchronization Input. Synchronize to an external clock with a frequency of 250kHz to 2.4MHz. Leave SYNC unconnected to disable the synchronization function.
29	FREQ	Oscillator Frequency Selection. Connect a resistor from FREQ to GND to select the switching frequency. See the *Frequency Select* section.
30	SYNCOUT	Oscillator Output. The SYNCOUT output is 180° out-of-phase from the internal oscillator or the SYNC signal to facilitate running a second regulator 180° out-of-phase with the first to reduce input ripple current.
31	GND	Analog Circuit Ground
32	FB	Feedback Input. Connect to the center tap of an external resistor-divider from the output to GND to set the output voltage.
—	EP	Exposed Paddle. Connect to a large ground plane for increased thermal performance.

High-Efficiency, 10A, PWM Internal-Switch Step-Down Regulator

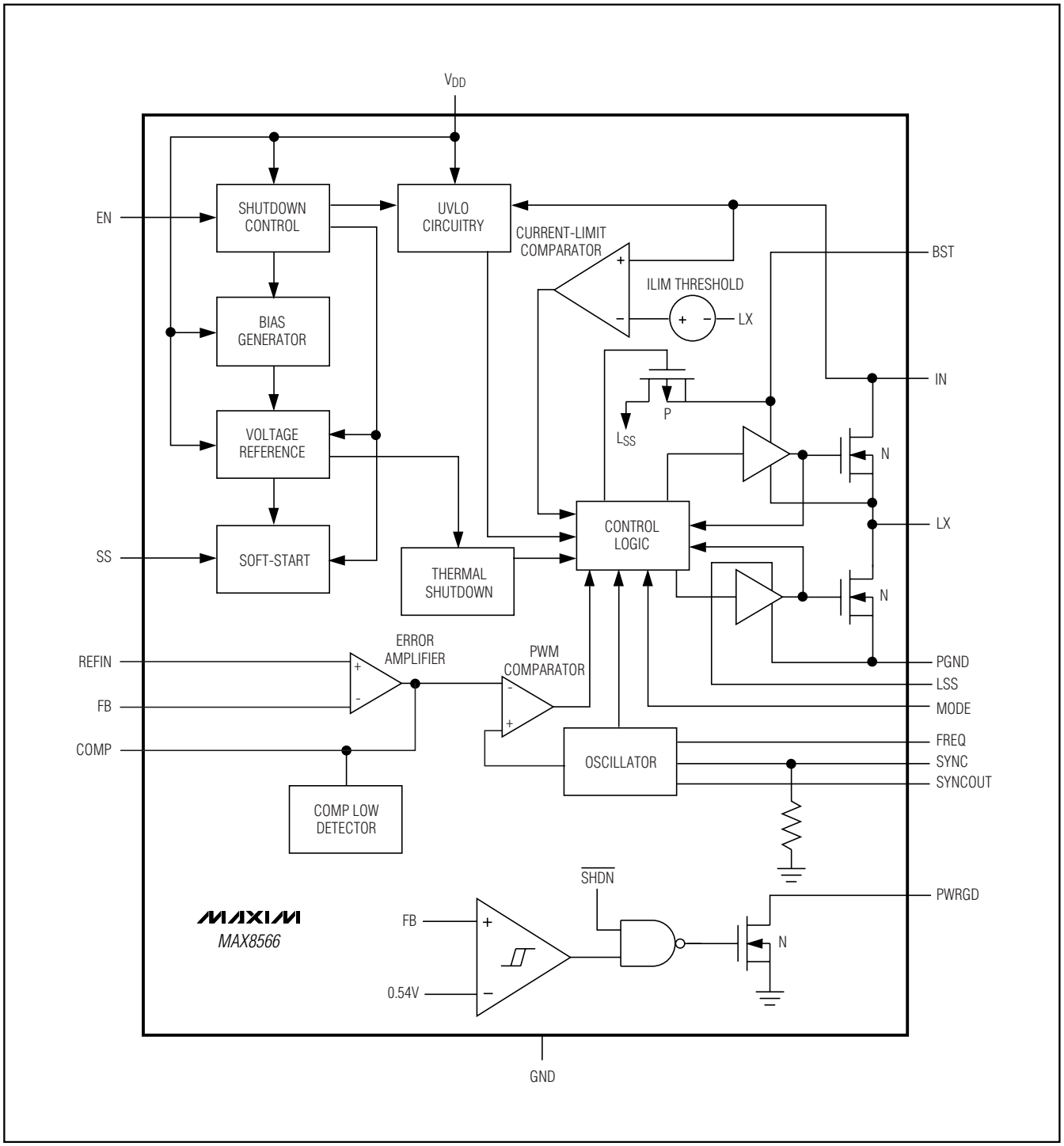


Figure 1. Functional Diagram

Detailed Description

The MAX8566 high-efficiency, voltage-mode switching regulator is capable of delivering up to 10A of output current. The MAX8566 provides output voltages from 0.6V to (0.87 x V_{IN}) from 2.3V to 3.6V input supplies, making it ideal for on-board point-of-load applications. The output voltage accuracy is better than ±1% over load, line, and temperature.

The MAX8566 features a wide switching frequency range, allowing the user to achieve all-ceramic-capacitor designs and faster transient responses. The high operating frequency minimizes the size of external components. The MAX8566 also features a wide 2.3V to 3.6V input voltage range, making it ideal for point-of-load applications with both 3.3V and 2.5V input voltages. The MAX8566 is available in a small (5mm x 5mm), 32-pin thin QFN package. The SYNCOUT function allows end users to operate two MAX8566s at the same switching frequency with 180° out-of-phase operation to minimize the input ripple current, consequently reducing the input capacitance requirements. The REFIN function makes the MAX8566 an ideal candidate for DDR and tracking power supplies. Using internal low-$R_{DS(ON)}$ (8mΩ) n-channel MOSFETs for both high- and low-side switches maintains high efficiency at both heavy-load and high-switching frequencies. In addition, the MAX8566 features a low-side-driver supply input (LSS) to boost the efficiency with a higher driver voltage (3.3V) for 2.5V input applications.

The MAX8566 employs the voltage-mode control architecture with a high bandwith (> 10MHz) error amplifier. The voltage-mode control architecture allows above 2MHz switching, reducing board area. The op-amp voltage error amplifier works with Type 3 compensation to fully utilize the bandwidth of the high-frequency switching to obtain fast transient response. Adjustable soft-start time provides flexibilities to minimize input startup inrush current. An open-drain power-good (PWRGD) output goes high when V_{FB} reaches 0.54V.

Principle of Operation

The controller logic block is the central processor that determines the duty cycle of the high-side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current limit and temperature protection are not triggered, the controller logic block takes the output from the PWM comparator and generates the driver signals for both high-side and low-side MOSFETs. The break-before-make logic and the timing for charging the bootstrap capacitors are calculated by the controller logic block. The error signal from the voltage error amplifier is compared with the ramp signal generated by the oscillator at the PWM comparator and thus the required PWM signal is produced. The high-side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the V_{COMP} signal or the current-limit threshold is exceeded. The low-side switch is then turned on for the remainder of the oscillator cycle.

Current Limit

The internal, high-side MOSFET has a typical 15A peak current-limit threshold. When current flowing out of LX exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. The synchronous rectifier remains on until the inductor current falls below the low-side current limit. This lowers the duty cycle and causes the output voltage to droop until the current limit is no longer exceeded.

The MAX8566 uses a hiccup mode to prevent overheating during short-circuit output conditions. The device enters hiccup mode when V_{FB} drops below 420mV and the current limit is reached. The IC turns off for 3.4ms and then enters soft-start. If the short-circuit condition remains after the soft-start time, the IC shuts down for another 3.4ms. The IC repeats this behavior until the short-circuit condition is removed.

Soft-Start and REFIN

The MAX8566 utilizes an adjustable soft-start function to limit inrush current during startup. An 8µA (typ) current source charges an external capacitor connected to SS to increase the capacitor voltage in a controlled manner. The soft-start time is adjusted by the value of the external capacitor from SS to GND. The required capacitance value is determined as:

$$C = \frac{8\mu A \times t_{SS}}{0.6V}$$

where t_{SS} is the required soft-start time in seconds.

The MAX8566 also features an external reference input (REFIN). The IC regulates FB to the voltage applied to REFIN. The internal soft-start is not available when using an external reference. A method of soft-start when using an external reference is shown in Figure 2. Connect REFIN to SS to use the internal 0.6V reference.

High-Efficiency, 10A, PWM Internal-Switch Step-Down Regulator

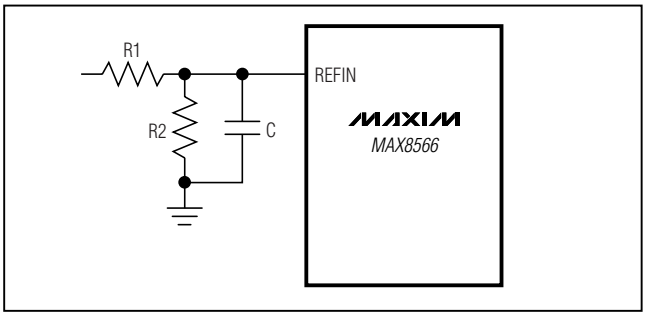


Figure 2. Soft-Start Implementation with External Reference

Undervoltage Lockout (UVLO)

The UVLO circuitry inhibits switching when V_{DD} is below 2V. Once V_{DD} rises above 2V, UVLO clears and the soft-start function activates. A 100mV hysteresis is built in for glitch immunity.

Monotonic Startup Modes (MODE)

When starting up into a precharged output, the MAX8566 does not discharge the output prior to entering soft-start (known as monotonic startup). Drive MODE to 1/3 of V_{DD} to enable monotonic startup mode. Connect MODE to GND to disable monotonic startup mode.

High-Side MOSFET Driver Supply (BST)

The gate-drive voltage for the high-side, n-channel switch is generated by a flying-capacitor boost circuit. The capacitor between BST and LX is charged from the V_{LSS} supply while the low-side MOSFET is on. When the low-side MOSFET is switched off, the stored voltage of the capacitor is stacked above LX to provide the necessary turn-on voltage for the high-side internal MOSFET.

Frequency Select (FREQ)

The switching frequency is resistor programmable from 250kHz to 2.4MHz. Set the switching frequency of the IC with a resistor from FREQ to GND (R_{FREQ}). R_{FREQ} is calculated as:

$$R_{FREQ} = \frac{50k\Omega}{0.95\mu s} \times \left(\frac{1}{f_S} - 0.05\mu s \right)$$

where f_S is the desired switching frequency in Hz.

SYNC Function (SYNC, SYNCOUT)

The MAX8566 features a SYNC function that allows the switching frequency to be synchronized to any frequency between 250kHz to 2.4MHz. Drive SYNC with a

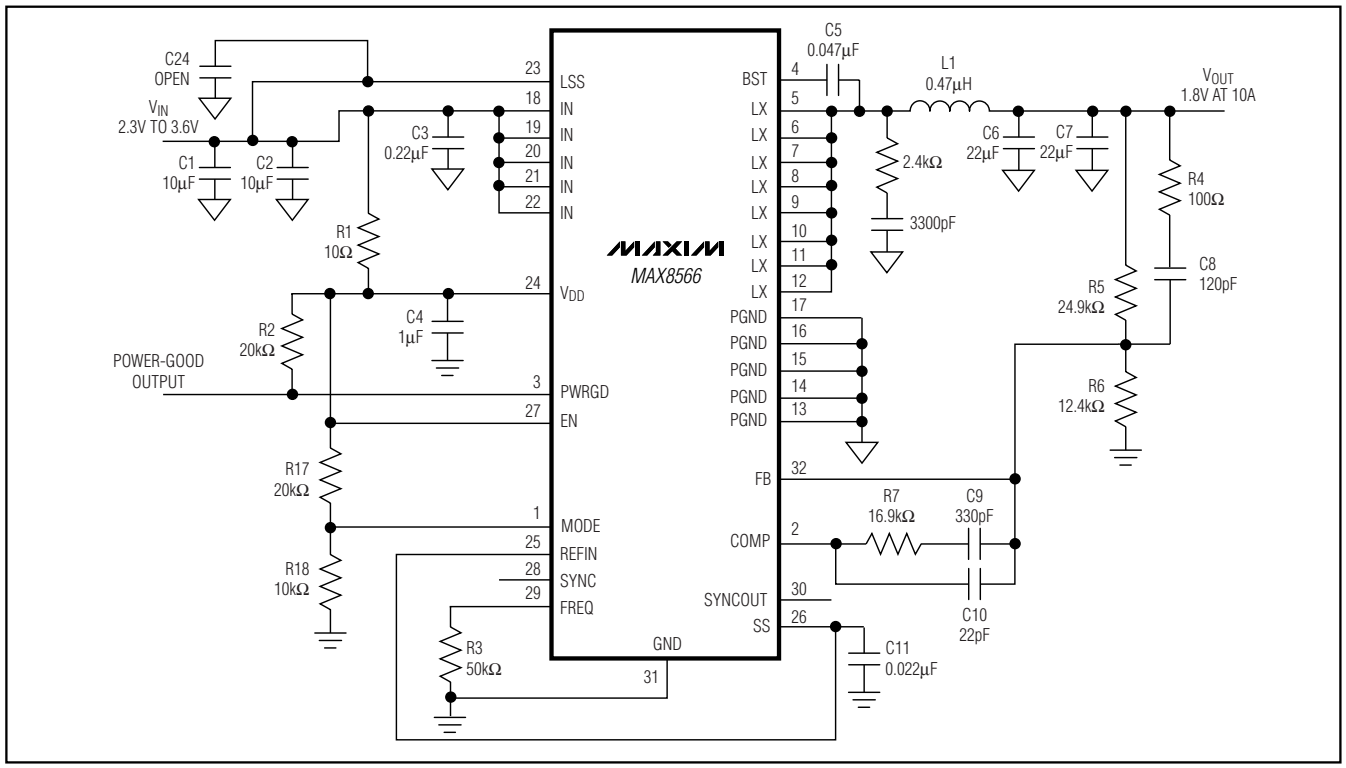


Figure 3. Typical Application Circuit.

square wave at the desired synchronization frequency. A rising edge on SYNC triggers the internal SYNC circuitry. The frequency of the input into SYNC must be higher than the internal oscillator frequency set by R_{FREQ}. Leave SYNC disconnected to disable the function and operate on the internal oscillator.

The MAX8566 has a SYNCOUT output that generates a clock signal that is 180° out-of-phase with its internal oscillator, or the signal applied to SYNC. This allows for another regulator to be synchronized 180° out-of-phase to reduce the input ripple current.

Power-Good Output (PWRGD)

PWRGD is an open-drain output that goes high impedance once the soft-start ramp has concluded, provided V_{FB} is above 0.54V. PWRGD pulls low when V_{FB} is below 0.54V for at least 50µs. PWRGD is low during shutdown.

Low-Side MOSFET Driver Supply (LSS)

The MAX8566 provides an external input for the low-side MOSFET driver supply (LSS). This allows for higher gate-drive voltages to maximize converter efficiency at low input voltages.

Shutdown Mode

Drive EN to GND to shut down the IC and reduce quiescent current to 4µA. During shutdown, the output is high impedance. Drive EN high to enable the MAX8566.

Thermal Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J = +165°C a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C, causing a pulsed output during continuous overload conditions. The soft-start sequence begins after a thermal-shutdown condition.

Applications Information

V_{DD} Decoupling

To decrease the noise effects due to the high switching frequency and maximize the output accuracy of the MAX8566, decouple V_{DD} with a 4.7µF capacitor from V_{DD} to GND and a 2Ω resistor from V_{DD} to V_{IN}. Place the capacitor as close to V_{DD} as possible.

Inductor Design

Choose an inductor with the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_S \times V_{IN} \times LIR \times I_{OUT(MAX)}}$$

where LIR is the ratio of the inductor ripple current to average continuous current at the minimum duty cycle. Choose the LIR between 20% to 40% for best performance and stability.

Use a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. Powered iron ferrite core types are often the best choice for performance. With any core material the core must be large enough not to saturate at the peak inductor current (I_{PEAK}). Calculate I_{PEAK} as follows:

$$I_{PEAK} = \left(1 + \frac{LIR}{2}\right) \times I_{OUT(MAX)}$$

Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Calculate the output voltage ripple due to the output capacitance, ESR, and ESL as:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL are:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{ON}} \times ESL$$

or $V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{OFF}} \times ESL$, whichever is greater.

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The peak inductor current (I_{P-P}) is:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Use these equations for initial capacitor selection. Determine final values by testing a prototype or an evaluation circuit. A smaller ripple current results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output voltage ripple decreases with larger inductance. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The low ESL of ceramic capacitors makes ripple voltages negligible.

Load-transient response depends on the selected output capacitance. During a load transient, the output instantly changes by ESR x I_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its predetermined value. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, preventing the output from deviating further from its regulating value. See the *Compensation Design* section for more details.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the IC. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source but are instead shunted through the input capacitor. High source impedance requires high input capacitance. The input capacitor must meet the ripple-current requirement imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RIPPLE} = I_{LOAD} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where I_{RIPPLE} is the input RMS ripple current.

Compensation Design

The power transfer function consists of one double pole and one zero. The double pole is introduced by the output filtering inductor, L, and the output filtering capacitor, C_O. The ESR of the output filtering capacitor determines the zero. The double pole and zero frequencies are given as follows:

$$f_{P1\_LC} = f_{P2\_LC} = \frac{1}{2\pi \times \sqrt{L \times C_O \times \left(\frac{R_O + ESR}{R_O + R_L}\right)}}$$

$$f_{Z\_ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

where R_L is equal to the sum of the output inductor's DCR and the internal switch resistance, R_{DSON}. A typical value for R_{DSON} is 8mΩ. R_O is the output load resistance, which is equal to the rated output voltage divided by the rated output current. ESR is the total equivalent series resistance of the output filtering capacitor. If there is more than one output capacitor of the same type in parallel, the value of the ESR in the above equation is equal to that of the ESR of a single output capacitor divided by the total number of output capacitors.

The high switching frequency range of the MAX8566 allows the use of ceramic output capacitors. Since the ESR of ceramic capacitors is typically very low, the frequency of the associated transfer-function zero is higher than the unity-gain crossover frequency, f_C, and the zero cannot be used to compensate for the double pole created by the output filtering inductor and capacitor. The double pole produces a gain drop of 40dB and a phase shift of 90 degrees per decade. The error amplifier must compensate for this gain drop and phase shift to achieve a stable high-bandwidth closed-loop system. Therefore, use Type 3 compensation as shown in Figure 4. Type 3 compensation possesses three poles and two zeros with the first pole, f_{P1_EA}, located at 0 frequency (DC). Locations of other poles and zeros of the Type 3 compensation are given by:

$$f_{Z1\_EA} = \frac{1}{2\pi \times R1 \times C1}$$

$$f_{Z2\_EA} = \frac{1}{2\pi \times R3 \times C3}$$

$$f_{P2\_EA} = \frac{1}{2\pi \times R1 \times C2}$$

$$f_{P3\_EA} = \frac{1}{2\pi \times R2 \times C3}$$

The above equations are based on the assumptions that C1>>C2, and R3>>R2, which are true in most applications. Placement of these poles and zeros is

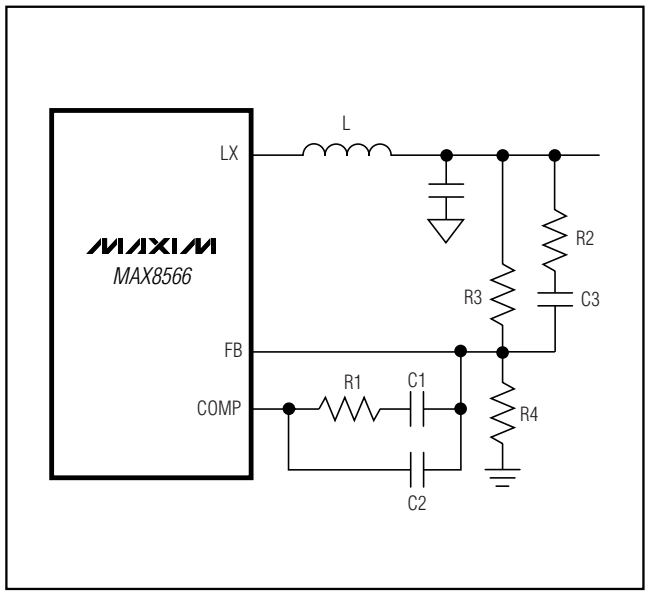


Figure 4. Type 3 Compensation Network

determined by the frequencies of the double pole and ESR zero of the power transfer function. It is also a function of the desired closed-loop bandwidth. The following section outlines the step-by-step design procedure to calculate the required compensation components.

Begin by setting the desired output voltage. The output voltage is set using a resistor-divider from the output to GND with FB at the center tap (R3 and R4 in Figure 4). Use 20kΩ for R4 and calculate R3 as:

$$R3 = R4 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right)$$

The zero-cross frequency of the closed-loop, f_C, should be less than 20% of the switching frequency, f_S.

Higher zero-cross frequency results in faster transient response. It is recommended that the zero-cross frequency of the closed loop should be chosen between 10% and 20% of the switching frequency. Once f_C is chosen, C1 is calculated from the following equation:

$$C1 = \frac{20 \times V_{IN}}{f_C \times 2 \times \pi \times R3 \times \left(1 + \frac{R_L}{R_O} \right)}$$

Due to the underdamped nature of the output LC double pole, set the two zero frequencies of the Type 3 compensation less than the LC double-pole frequency to provide adequate phase boost. Set the two zero frequencies to 80% of the LC double-pole frequency. Hence:

$$R1 = \frac{1}{0.8 \times C1} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

$$C3 = \frac{1}{0.8 \times R3} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

Set the second compensation pole, f_{P2_EA}, at f_{Z_ESR} yields:

$$C2 = \frac{C_O \times C1 \times ESR}{R1 \times C1 - C_O \times ESR}$$

Set the third compensation pole at 1/2 of the switching frequency to gain some phase margin. Calculate R2 as follows:

$$R2 = \frac{1}{\pi \times C3 \times f_S}$$

The above equations provide accurate compensation when the zero-cross frequency is significantly higher than the double-pole frequency. When the zero-cross frequency is near the double-pole frequency, the actual zero-cross frequency is higher than the calculated frequency. In this case, lowering the value of R1 reduces the zero-cross frequency. Also, set the third pole of the Type 3 compensation close to the switching frequency if the zero-cross frequency is above 200kHz to boost the phase margin. Please note that the value of R4 can be altered to make the values of the compensation components practical. The recommended range for R4 is 10kΩ to 50kΩ.

PC Board Layout Considerations and Thermal Performance

The MAX8566EVKIT provides an optimal layout and should be followed closely. For custom design, follow these guidelines:

1) Place decoupling capacitors (V_{DD} and SS) as close to the IC as possible. Keep the power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.

High-Efficiency, 10A, PWM Internal-Switch Step-Down Regulator

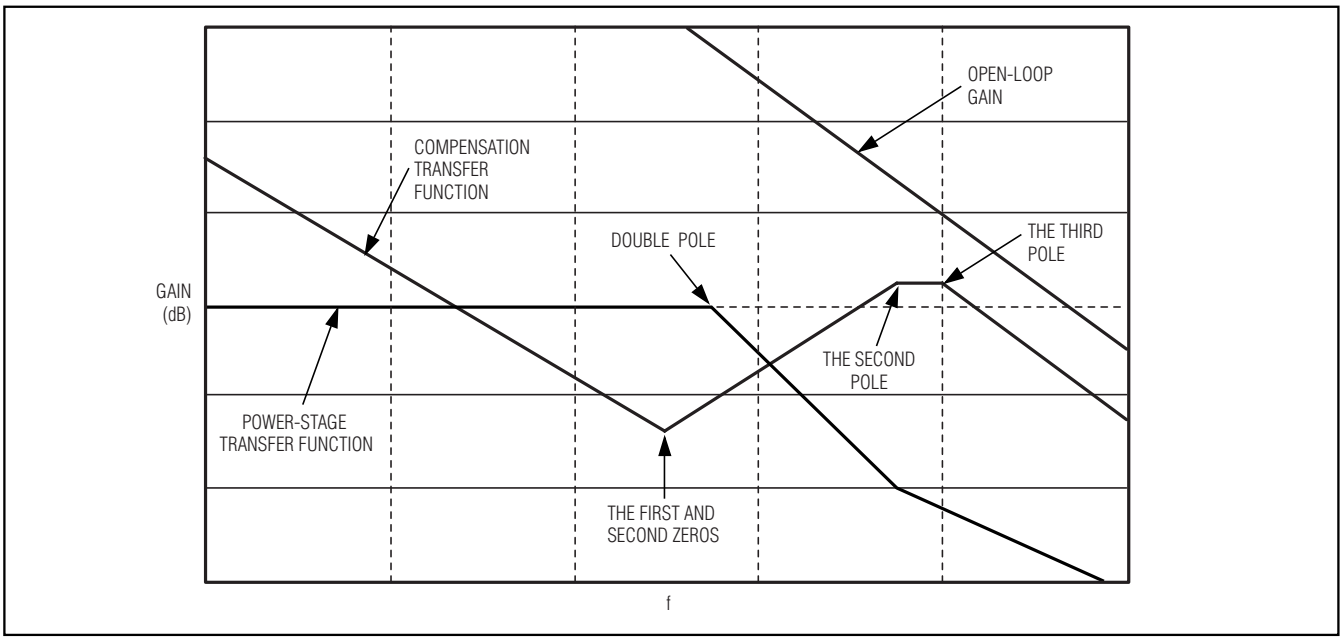
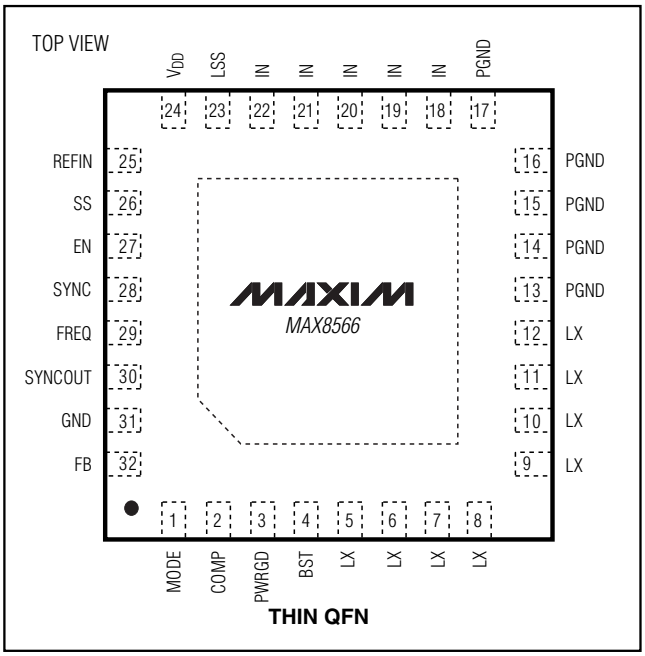


Figure 5. Transfer Function for Type 3 Compensation

2) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4) Connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the IC as possible.
6) Route high-speed switching nodes away from sensitive analog areas (FB, COMP).

High-Efficiency, 10A, PWM Internal-Switch Step-Down Regulator

Pin Configuration



Chip Information

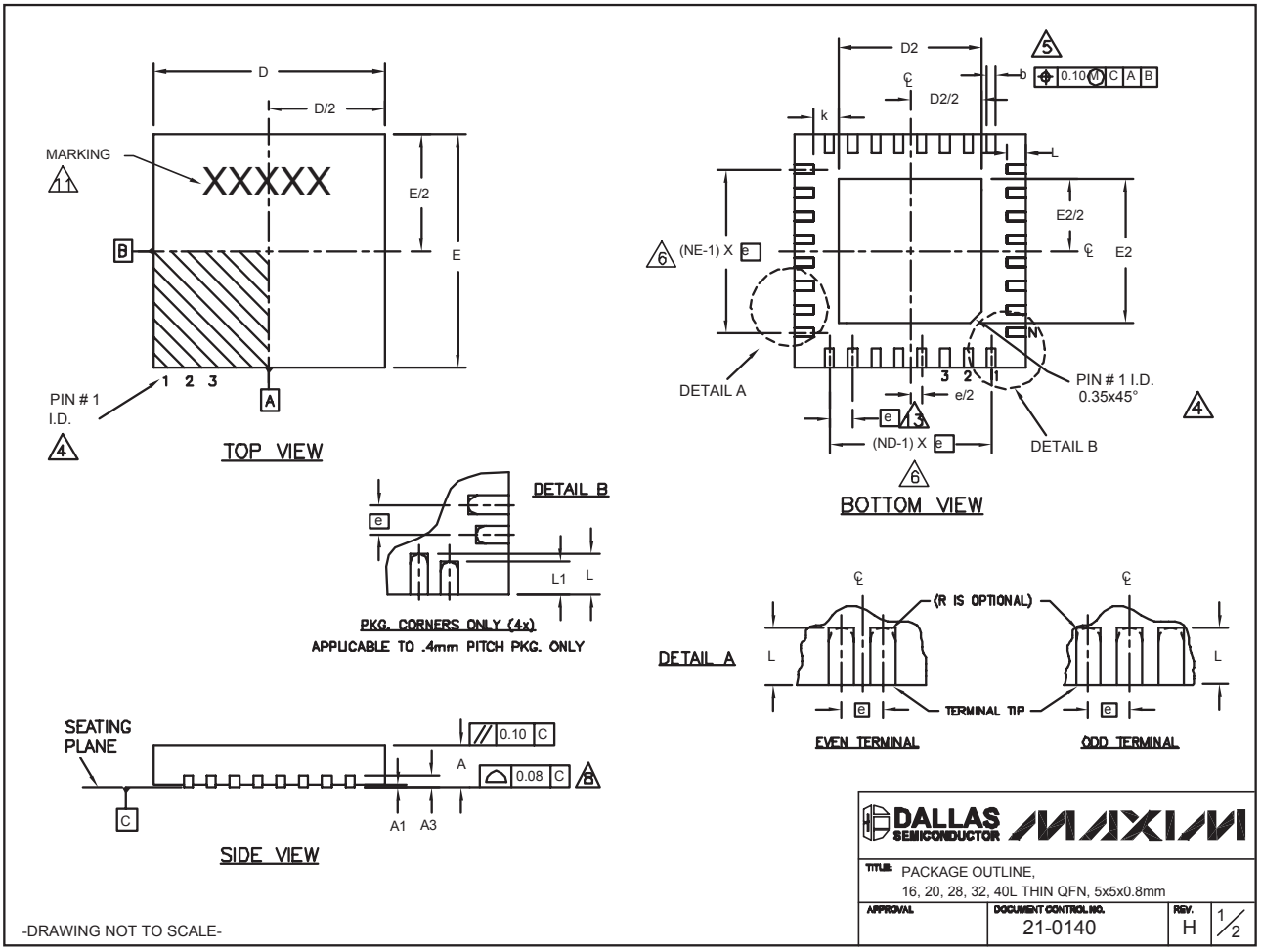
PROCESS: BiCMOS

High-Efficiency, 10A, PWM Internal-Switch Step-Down Regulator

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

** SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3, AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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